REMARKS

The Final Office Action mailed December 31, 2002, has been received and reviewed. Claims 1 through 20 are currently pending in the application. Claims 1 through 20 stand rejected. Applicants respectfully request reconsideration of the application in view of the discussion below.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,147,413 to Farnworth in view of U.S. Patent No. 5,894,107 to Lee et al.

Claims 1 through 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Farnworth (U.S. Patent No. 6,147,413) in view of Lee et al. (U.S. Patent No. 5,894,107). Applicants respectfully traverse this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
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> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness type rejection of claims 1 through 20 is improper because it fails to establish a *prima facie* case of obviousness.

Turning to the cited references, Farnworth describes a method of forming conductive bumps on a die for flip chip type attachment using simplified masking steps. In the method, a first polyamide passivation layer 1006 is applied to a wafer active surface 1010 by spin coating (col. 4, lines 3-10). A via 1008 is etched through passivation layer 1006 to expose bond pad 1002 (col. 4, lines 27-32). A conductive layer 1012 is then deposited over passivation layer 1006 and masked and etched to form repattern trace 1016 which extends to an alternative bond pad location (col. 4, lines 39-44). A second passivation layer 1018 is spun-on over repattern trace

1016, and a via 1026 is formed therein to connect a solder ball 1032 to the alternative bond pad location of repattern trace 1016 (col. 4, line 45 - col. 5, line 40).

Lee et al. teaches a prior art chip-size package that uses half etched leads 76 to connect to bonding pads 74. (Fig. 1 and cols. 1 and 2). Leads 76 are attached to an active surface of semiconductor chip 72 by adhesive tape 78, and bonding pads 74 are connected to leads 76 with wires 80 (col. 1, line 66 - col. 2, line 1). The assembly is encapsulated with epoxy molding compound 82 such that bonding pads 74 and wires 80 are protected from the external environment, while the thick portions of leads 76 are exposed to the outside (col. 2, lines 1-8).

In rejecting claims 1 through 20, the Office asserts that Farnworth discloses all of the elements of the claims except the discrete conductive bond. The Office then concludes that it would be obvious to combine Lee et al. with Farnworth, and that Lee et al. is "only cited to teach the well known discrete bond." (Office Action mailed 12/31/2002, paper no. 16 at page 4, lines 7-8.) The fact that bond wires such as those taught by Lee et al. are known in the art, does not mean that bond wires may be incorporated into the structure disclosed by Farnworth. Instead, Applicants respectfully submit that combining Farnworth and Lee et al. in such a manner is improper and does not satisfy the requirements of an obviousness-type rejection under 35 U.S.C. § 103(a).

First, the Office suggests that it would be obvious to "modify the conductive trace configuration of Farnworth by employing a lead on chip configuration as taught by Lee to increase the package density and provide better electrical performance." Due to the differences in structure and scale between the repattern traces of Farnworth and the wires of Lee et al., Applicants submit there is no support for this line of reasoning.

Farnworth is directed generally to repatterning of flip chip or BGA type bond locations on a semiconductor die and more specifically to forming the repattern traces with reduced masking steps (col. 1, lines 14-22). Contrary to the suggestion of the Office, employing the bond wires of Lee et al. with the repattern structures of Farnworth would not increase package density. Repattern traces for flip chip or BGA structures as described in Farnworth are formed by masking and etching an under bump metallization that is adhered in a thin layer to the surface of the underlying passivation layer (col. 4, lines 33-44). Bond wires used in lead on chip

configurations, on the other hand, are well known as extending between bonding locations in elevated, arched configurations (see Lee et al, Fig. 1). Adding bond wires to the repattern structure of Farnworth would, therefore, **require an enlarged packaged size** to accommodate the height of the bond wires within the passivation layer 1018.

Furthermore, bond wires would not provide better electrical performance, as suggested by the Office, but would instead **decrease electrical performance**. The bond wires would add length to the conductive pathway between bond pad 1002 and solder ball 1032, thereby increasing electrical resistance and the possibility of interference from inductance generated signal noise. It is also well known in the art that attaching bond wires is difficult and must be carried out under tightly controlled processing conditions. Adding bond wires to the repattern structure of Farnworth would raise the possibility of improper bond wire attachment degrading the electrical performance.

Moreover, Applicants respectfully submit that Farnworth teaches away from any combination with Lee et al. Farnworth indicates an object of the invention is to simplify or eliminate masking steps in UBM pad forming when repatterning bond pad locations (Abstract and col. 1, lines 14-22). In its present form, the invention described by Farnsworth allows the repattern trace 1016 connecting bond pad 1002 and solder ball 1032 to be formed with a single mask and etch step (col. 4, lines 39-44). In order to include an intermediate bond wire between repattern trace 1016 and bond pad 1002, **additional or more complicated masking steps would be required**. Further process steps would also be necessary in terms of connecting trace 1016 and bond pad 1002 with a bond wire instead of directly connecting them.

In sum, there is no reasonable basis for why one of ordinary skill in the art would be motivated to modify the repattern structure of Farnworth with the bond wires of Lee et al., when doing so would increase the package size, reduce performance and complicate the formation process. Rather than presenting a valid motivation for the above combination, Applicants respectfully submit that the Office has merely attempted to piece together the claimed invention with the hindsight benefit of Applicants' own disclosure. The Federal Circuit has repeatedly cautioned against employing hindsight by using the applicant's disclosure as a blueprint to

reconstruct the claimed invention out of isolated teaching of the prior art. *See, e.g., Grain Processing Corp. v. American-Maize Prods. Co.*, 5 U.S.P.Q.2d 1788, 1792 (Fed. Cir. 1988).

Even if some motivation could be found for adding bond wires to the structure of Farnworth, there is no reasonable expectation of success for the combination, as the trace formation process used in Farnworth is not compatible with bond wires. As described above, Farnworth uses a series of mask, etch and spin coat steps to form via 1008 and repattern trace 1016 and to cover the trace configuration with passivation layer 1018 (Farnworth at col. 4). It is unclear how these steps could be carried out in the presence of bond wires. At the least, the process described by Farnworth **would require major alterations to provide the proposed combination**, rendering it non-obvious.

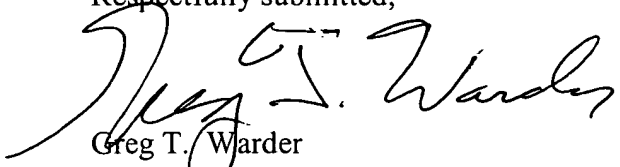
Finally, the combination of Farnworth and Lee et al. as presented by the Office does not teach or suggest all the claim limitations. Claim 3, for instance, recites the limitation "wherein said dielectric element includes an adhesive-coated polyimide tape." Farnworth, on the other hand, does not disclose an adhesive-coated polyimide tape, but instead uses a polyamide layer 1006 applied by spin coating (col. 4, lines 1-26). Likewise, claim 6 recites that "said plurality of conductive traces comprises lead fingers." The repattern traces of Farnworth are not comprised of lead fingers, but instead comprise a conductive layer 1012 of solder wettable metal applied over polyamide layer 1006 and etched into repattern traces 1016 (col. 4, lines 33-48). Claims 11 and 12 further recite discrete conductive elements comprised of "TAB bonds" or "thermocompression bonds." Farnworth does not disclose such structures. Claim 14 recites a plurality of carrier bonds comprised of a "conductive or conductor-filled polymer. Farnworth is limited to a description of a solder ball 1032 (col. 5, lines 38-40). The citation of Lee et al. to add bond wires to the repattern structure of Farnworth does not overcome these deficiencies.

In view of the foregoing, Applicants respectfully submit that the combination of Farnworth with Lee et al. as presented does not establish a prima facie case of obviousness under 35 U.S.C. § 103(a), and respectfully request the rejection of claims 1 through 20 be withdrawn.

CONCLUSION

Claims 1 through 20 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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